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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
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| 09/943,094 | 08/29/2001 | Kazunobu Kuwazawa | 81751.0017 | 7672 |

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| EXAMINER | |
|---|---|
| SEFER, AHMED N | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2826 | |

DATE MAILED: 06/10/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 09/943,094 | KUWAZAWA, KAZUNOBU | |
| | Examiner | Art Unit | |
| | A. Sefer | 2826 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *13 March 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

NATHAN J. FLYNN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

**Priority under 35 U.S.C. §§ 119 and 120**

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____.
4) ☐ Interview Summary (PTO-413) Paper No(s). _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

## DETAILED ACTION

### *Response to Amendment*

1. The amendment filed on 3/13/03 has been entered; no new claims have been added. Applicant is reminded that claims 20-31 have been cancelled (see Paper No. 7) and only claims 1-19 are pending.

### *Claim Rejections - 35 USC § 102*

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in-
> (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effect under this subsection of a national application published under section 122(b) only if the international application designating the United States was published under Article 21(2)(a) of such treaty in the English language; or
> (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that a patent shall not be deemed filed in the United States for the purposes of this subsection based on the filing of an international application filed under the treaty defined in section 351(a).

3. Claims 1-3 are rejected under 35 U.S.C. 102(b) as being anticipated by Wakahara et al. (JP 11-54758).

Wakahara et al disclose in fig. 2 a semiconductor substrate 1a having a first conductive layer 14 functioning as a wiring layer (as in claim 3) formed from an impurity layer (as in claim 2) provided therein; an insulation layer 1b provided above the semiconductor substrate; a semiconductor layer 1c provided above the insulation layer, wherein the semiconductor layer includes an element isolation region 2a which has a connection hole 11d; and a second

conductive layer 12d provided above the semiconductor layer, and electrically connected to the first conductive layer; and a contact layer (unnumbered) provided in the connection hole, the contact layer electrically connecting the first conductive layer and the second conductive layer.

4. Claims 1, 2 and 4 are rejected under 35 U.S.C. 102(e) as being anticipated by Matsumoto US Patent No. 6,372,562.

Matsumoto discloses (see figs. 1-4 and col. 6, lines 5-9) a semiconductor substrate 1 having a first conductive layer 11 functioning as a resistance layer (as in claim 4) formed an impurity layer (as in claim 2) provided therein; an insulation layer 2 provided above the semiconductor substrate; a semiconductor layer 3 provided above the insulation layer, wherein the semiconductor layer includes an element isolation region 4 which has a connection hole 10; and a second conductive layer (unnumbered) provided above the semiconductor layer, and electrically connected to the first conductive layer; and a contact layer (unnumbered) provided in the connection hole, the contact layer electrically connecting the first conductive layer and the second conductive layer.

5. Claims 1, 2 and 4 are rejected under 35 U.S.C. 102(e) as being anticipated by Ko et al. US Patent No. 6,407,429.

Ko et al disclose (see figs. 2 and 4, abstract and col. 11, lines 40-45) a semiconductor substrate 100a having a first conductive layer 134/128 functioning as a resistance layer (as in claim 4) formed from an impurity layer (as in claim 2) provided therein; an insulation layer 100b provided above the semiconductor substrate; a semiconductor layer 100c provided above the insulation layer, wherein the semiconductor layer includes an element isolation region 102 which has a connection hole; and a second conductive layer 142 provided above the semiconductor

layer, and electrically connected to the first conductive layer; and a contact layer (unnumbered) provided in the connection hole, the contact layer electrically connecting the first conductive layer and the second conductive layer.

6. Claims 7, 8 and 12 are rejected under 35 U.S.C. 102(e) as being anticipated by Matsumoto US Patent No. 6,372,562.

Matsumoto discloses (see figs. 1-4 and col. 6, lines 5-9) a semiconductor substrate 1 having a contact region 11 formed from an impurity layer (as in claim 8) provided therein; an insulation layer 2 provided above the semiconductor substrate; and a semiconductor layer 3 provided above the insulation layer, wherein the semiconductor layer includes an element isolation region 4 which has a connection hole 10; a conductive layer (unnumbered) provided above the semiconductor layer, and the contact region being electrically connected to the conductive layer; and a contact layer (unnumbered) provided in the connection hole, the contact layer electrically connecting the contact region and the conductive layer.

As to the intended function of the said conductive layer, a recitation of the intended use of the claimed invention must result in a structural difference between the claimed invention and the prior art in order to patentably distinguish the claimed invention from the prior art. If the prior art structure is capable of performing the intended use, then it meets the claim. See In re Casey, 152 USPQ 235 (CCPA 1967) and In re Otto, 136 USPQ 458, 459 (CCPA 1963).

As to claim 12, Matsumoto discloses a connection hole for connecting the contact region to the conductive layer, and wherein a contact layer is provided in the connection hole.

7. Claims 7, 8 and 12 are rejected under 35 U.S.C. 102(b) as being anticipated by Wakahara et al. (JP 11-54758).

Wakahara et al disclose in fig. 2 a semiconductor substrate 1a having a contact region 14 formed from an impurity layer (as in claim 8) provided therein; an insulation layer 1b provided above the semiconductor substrate; a semiconductor layer 1c provided above the insulation layer, wherein the semiconductor layer includes an element isolation region 2a which has a connection hole 11d; and a conductive layer 12d provided above the semiconductor layer; and the contact region being electrically connected to the conductive layer; and a contact layer (unnumbered) provided in the connection hole, the contact layer electrically connecting the contact region and the conductive layer.

As to the intended function of the said conductive layer, a recitation of the intended use of the claimed invention must result in a structural difference between the claimed invention and the prior art in order to patentably distinguish the claimed invention from the prior art. If the prior art structure is capable of performing the intended use, then it meets the claim. See In re Casey, 152 USPQ 235 (CCPA 1967) and In re Otto, 136 USPQ 458, 459 (CCPA 1963).

As to claim 12, Wakahara et al disclose a connection hole for connecting the contact region to the conductive layer, and wherein a contact layer is provided in the connection hole.

8. Claims 7-11 are rejected under 35 U.S.C. 102(e) as being anticipated by Ko et al. US Patent No. 6,407,429.

Ko et al disclose (see figs. 2 and 4, abstract and col. 11, lines 40-45) semiconductor device comprising a semiconductor substrate 100a or p-type substrate (as in claim 11) having a contact region 128 formed from an impurity layer (as in claim 8) or n-type contact region (as in claim 11) provided therein; an insulation layer 100b provided above the semiconductor substrate; and a semiconductor layer 100c provided above the insulation layer, wherein the semiconductor

layer includes an element isolation region 102 which has a connection hole; and a conductive layer 142 provided above the semiconductor layer, and has a function of allowing charge to flow into the semiconductor substrate, the contact region being electrically connected to the conductive layer; and a contact layer (unnumbered) provided in the connection hole, the contact layer electrically connecting the contact region and the conductive layer.

As to claim 9, Ko et al disclose a pn junction formed by the contact region and the semiconductor substrate.

As to claim 10, Ko et al disclose an n-type semiconductor substrate 104 and a p-type contact region 134.

9. Claims 14-16 are rejected under 35 U.S.C. 102(b) as being anticipated by Morihara US Patent No. 5,888,854.

Morihara discloses in figs. 42 and 43 a semiconductor device comprising a semiconductor substrate 1 having a first electrode 80 formed from a first impurity layer (as in claim 15) provided therein; an insulation layer 2 provided above the semiconductor substrate; a semiconductor layer 8 provided above the insulation layer, the semiconductor layer having a second electrode 8a/8c formed from a second impurity layer (as in claim 16) provided therein; and the first electrode, the second electrode, and the insulation layer in cooperation turning a capacitive element 15.

10. Claims 14-18 are rejected under 35 U.S.C. 102(b) as being anticipated by Wakahara et al. (JP 11-54758).

Wakahara et al. disclose in fig. 2 a semiconductor device comprising a

semiconductor substrate 1a having a first electrode 14 formed from a first impurity layer (as in claim 15) provided therein; an insulation layer 1b provided above the semiconductor substrate; a semiconductor layer 1c provided above the insulation layer, the semiconductor layer having a second electrode 13 formed from a second impurity layer (as in claim 16) provided therein; and the first electrode, the second electrode, and the insulation layer in cooperation turning a capacitive element.

As to claim 17, Wakahara et al disclose a first electrode connected electrically to a conductive layer 12d provided above the semiconductor layer.

As to claim 18, Wakahara et al disclose a connection hole 11d provided for connecting the first electrode layer to the conductive layer.

### *Claim Rejections - 35 USC § 103*

11. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

12. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Matsumoto in view of Yoshida (JP 2000-216400).

Matsumoto discloses the device structure as recited in the claim, but does not specifically disclose a connection hole that extends into a semiconductor substrate.

Yoshida discloses (see fig. 4 and abstract) a connection hole 4 that extends into a semiconductor substrate 1.

Therefore, it would have been obvious to one skilled in the art at the time the invention was made to incorporate the teachings of Yoshida with the device of Masumoto since that would provide a reliable connection between a connection area and a substrate.

13. Claims 6, 13 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wakahara et al in view of Drynan US Patent No. 6,511,879.

Wakahara et al disclose the device structure as recited in the claim, but do not specifically disclose a side wall provided in a connection hall.

Drynan discloses (see figs. 13 and 14, col. 3, lines 10-18 and col. 5, lines 25-33) a side wall 34 provided in a connection hall 30.

Therefore, it would have been obvious to one skilled in the art at the time the invention was made to incorporate Drynan's teachings with the device of Wakahara et al since that would prevent unintended shorting.

***Conclusion***

14. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

a. Masuda (JP 2000196102) disclose an SOI device with a metal electrode formed in the contact holes penetrating the insulating and oxide films.

b. Kim (JP 2001-94061) discloses an IC device having a resistance diffusion region formed under a plurality of MOS transistors isolated by an insulating film.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to A. Sefer whose telephone number is (703) 605-1227

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan Flynn can be reached on (703) 308-6601.

ANS
May 27, 2003